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(71) Applicant: **International Business Machines Corporation**
Old Orchard Road
Armonk, N.Y. 10504 (US)

(72) Inventor: **Sawdon, David**
29 Pine Close,
South Wonston
Winchester, Hampshire SO21 3EB (GB)

(74) Representative: **Williams, Julian David**
IBM United Kingdom Limited,
Intellectual Property Department,
Hursley Park
Winchester, Hampshire SO21 2JN (GB)

(54) Display system.

(57) A display system is described, comprising a display device (88) for generating a visual output in response to a plurality of data signals defining the data to be displayed, a display adapter circuit (92) for generating the data signals in a form specified by control data identifying the display device (88), an output port (94) for connecting the data signals from the display adapter circuit to the display device (88) and for connecting the control data from the display device (88) to the display adapter circuit (92), characterised in that the display system further comprises a non-volatile memory (9) located in the display device (88) for storing the control data in the form of a plurality of control codes, and communication logic (95) for communicating a control code between the memory and the output port (94) in response to a command signal (21) generated by the display adapter circuit (92). The communication logic comprises a serial data link (3) for communicating the control code between the display device and the output port, device logic (97) located in the display device for communicating the control code between the memory and the serial data link, and adapter logic (96) located in the display adapter circuit for communicating the control code between the serial data link and the display adapter circuit. The control data, such as the signal timing requirements of any new display device, can be stored in the form of digital control codes held within the memory of the display device, the display system programming does not require updating every time a different display device is connected to the output port. Instead, the display adaptor can read the new timing requirements from the memory of the new display device for the purpose of generating video and sync signals for correctly driving the new display device. Furthermore, where the display system comprises a multiple mode display device, the display adapter circuit can use the serial link to configure the display device to operate in a desired display mode.

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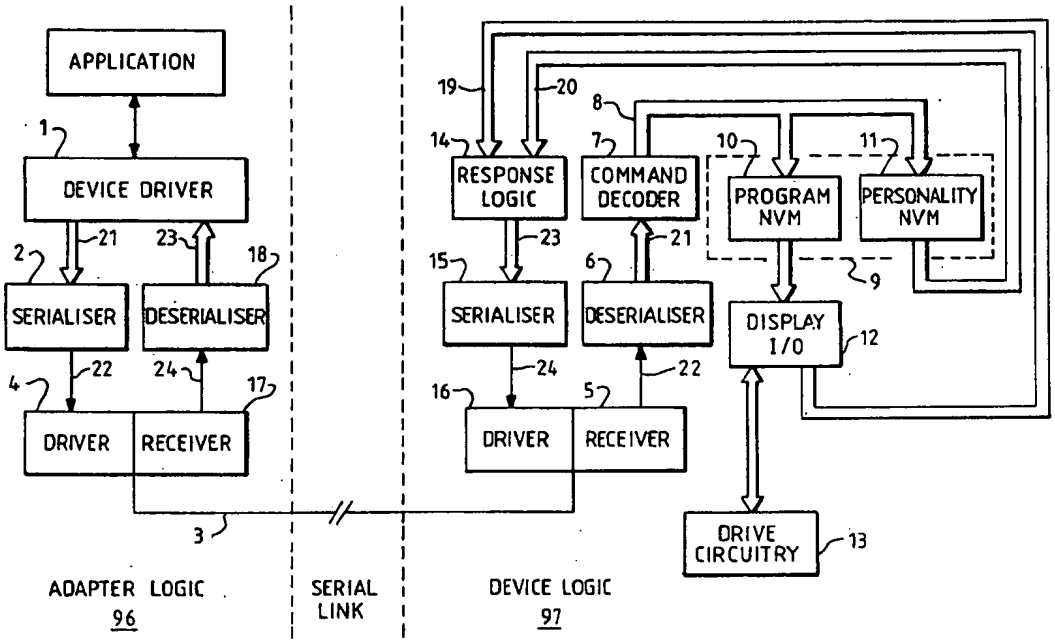
APPLICATION
1
DEVICE DRIVER
2
21
23
18
SERIALISER
DESERIALISER
4
22
24
17
DRIVER
RECEIVER
3
ADAPTER LOGIC
96
SERIAL
LINK
19
20
8
14
7
10
11
RESPONSE
LOGIC
COMMAND
DECODER
PROGRAM
NVM
PERSONALITY
NVM
23
21
9
15
6
SERIALISER
DESERIALISER
DISPLAY
I/O
12
24
22
16
5
DRIVER
RECEIVER
DRIVE
CIRCUITRY
13
DEVICE LOGIC
97

FIG. 2

The present invention is related to a display system in which control data is communicated between a computer system and a display device.

The control data includes parameters for specifying the geometry and resolution of an image presented on the display device. In a display system comprising a raster-scanned display device such as a Cathode Ray Tube (CRT) display device, these parameters are determined by the rates and amplitudes of horizontal and vertical scan signals generated for producing the raster scan by electrical circuits in the display device. In order to generate the image, the scan signals are synchronised to video signals from a video source such as a computer system by synchronisation (sync) pulses also generated by the video source.

Some display devices can only operate in a single display mode in accordance with a single set of parameters. Other display devices can be configured to operate in any one of a number of display modes characterised by different sets of parameters. The latter will hereinafter be referred to as multiple mode display devices. In a display device controlled by a computer system it is desirable for the computer system to identify the type of the display device so that appropriate video and sync signals can be generated. Many examples of such computer systems, including the IBM PS 2 range, comprise a video graphics adapter (VGA adapter) having an output port for connecting video and sync signals to a display device. The VGA adapter also has logic responsive to the manner in which identification pins in the output port are terminated when connected to the display device. The logic identifies the type of display device connected to the VGA adapter from these terminations.

UK Patent No 2,162,026 describes an example of a display system employing a multiple-mode display device receiving video and sync signals from a computer system display adapter. The display device can operate in any one of four display modes. The computer system can be instructed to provide sync pulses of either positive or negative polarities. Each polarity combination indicates a different display mode. The display device includes decoding logic for configuring the display device to operate in a particular display mode in response to predetermined sync pulse polarities.

The display systems of the prior art have the disadvantage that the display interfaces of the prior art can identify, and therefore generate appropriate control signals for, only a limited number of different display devices. This limitation arises because the number of pins available for display device identification and control is limited by the physical form of the output port.

In accordance with the present invention, there is now proposed a display device for connection to a display adaptor circuit of a computer system, the display device comprising: means for generating a visual output in response to a plurality of data signals generated by the display adaptor circuit; characterised in that the display device comprises: a memory to store control data in the form of a plurality of control codes identifying the display device; and device logic means responsive to a command signal from the display adaptor circuit to read control codes from the memory for transfer to the display adaptor circuit. This has the advantage that, since the control data such as the signal timing requirements of any new display device can now be stored in the form of digital control codes held within the memory of the display device, the display system programming does not require updating every time a different display device is connected to the output port. Instead, the display adapter can now read the new timing requirements from the memory of the new display device for the purpose of generating video and sync signals for correctly driving the new display device.

Preferably, the display device comprises serial data link means for communicating the control code between the display device and the adapter circuit. This has the advantage that, where the display device is a multiple mode display device, the display adapter circuit can use the serial link to configure the display device to operate in a desired display mode.

An example of the present invention will now be described with reference to the accompanying drawings in which:

Figure 1 is a block diagram of a computer system incorporating a display system including a display device; and

Figure 2 is a block diagram of communication logic for communicating display information between the display adapter and the display device.

Figure 1 illustrates an example of a computer system incorporating a display system having a CRT display device 88.

The computer system includes a central processing unit (CPU) 80 for executing programmed instructions. A bus architecture 86 provides a data communication path between the CPU 80 and other components of the display system. A read only memory (ROS) 81 provides secure storage of data. A random access memory 82 provides temporary data storage. Data communication with a host computer system 93 is provided by a communication adapter 85. An I/O adapter 84 enables data to pass between the bus architecture 86 and a peripheral device such as a disk file 83. A user can operate the computer system using a keyboard 91 which is connected to the bus architecture 86 by a keyboard adapter 90. The CRT display device 88

provides a visual output from the display system. A display adapter 92 generates video and sync signals at an output port 94 for enabling the display device 88 to generate the visual output.

In accordance with the present invention, the display device 88 comprises a Non-Volatile Memory (NVM) 9 for storing display information in the form of digital codes. The display information is communicated between the display device 88 and the display adapter 92 along a serial link 3 which is controlled by Communication logic 95. The serial link 3 is separate from the lines carrying the video and sync signals from the display adapter 92 to the display device. The communication logic 95 is divided into adapter logic 96 and device logic 97. In operation, the adapter logic 96 initiates commands for both reading and writing data to the NVM 9 and the device logic 97 responds accordingly.

The communication logic 95 will now be described in further detail with reference to Figure 2. The adapter logic 96 comprises a device driver 1 for generating a command code 21 in response to a program instruction. A first serialiser 2 translates the command code 21 into a command bit stream 22 for a first line driver 4 to communicate to the device logic 97 along the serial link 3. The device logic 97 comprises a second receiver 5 for detecting the command bit stream 22. A second deserialiser 6 translates the command bit stream 22 back into the command code 21. A command decoder 7 decodes the command code 21 into an NVM address 8. Address space in the NVM 9 is divided into a personality NVM 10 and a program NVM 11.

The personality NVM 10 contains identification codes for providing the display system with a specification of the display device 88 connected to the display adapter 92. Each identification code is stored in a different address location. The identification codes include coded timing parameters for enabling the display adapter 92 to generate appropriate video and sync signals. Specifically, the timing parameters include sync pulse widths, active video periods, and blanking intervals. Preferably, the identification codes also include a coded transfer parameter for indicating the maximum rate at which the device logic 97 can read or write data to the serial link 3. By reading the transfer parameter before issuing any further commands, the adapter logic 96 can ensure that data is subsequently transferred between the display device 88 and the display adapter 92 at a rate which is compatible with both the adapter logic 96 and the device logic 97. Each timing parameter is stored in the form of a sixteen bit identification code. Fifteen bits of the code specify the value of the timing parameter and the sixteenth bit specifies the polarity. It will be appreciated that less critical timing parameters may be stored in the form of eight bit codes or less. The personality NVM stores several sets of timing parameters corresponding to different display modes of the display device.

The program NVM 11 stores control codes for instructing a display input/output (I/O) circuit 12 to adjust drive signals generated by drive circuitry 13 in the display device. Examples of such drive signals directly affect the height, width, and brightness of the visual output from the display device 88. Each control code is stored in a different address location. By instructing the display I/O circuit 12 with appropriate control codes, the visual output of the display device 88 can be switched between different display modes under the control of a computer program. Preferably the program NVM 11 also stores control codes for instructing the display I/O circuit 12 to generate sample codes representative of drive signal magnitudes at predetermined nodes of the drive circuitry 13. It will be appreciated that such control codes may be used to automate diagnostic methods for testing the operation of the display device 88 after manufacture or repair.

When the adapter logic 96 issues a read command, the device logic 97 responds by placing an appropriate response code 23 on the serial link 3. The response code 23 may either be an identification code 20 from the personality NVM or a sampled data code 19 from the display I/O circuit 12 depending on the nature of the read command. For implementing such a response, the device logic 97 comprises parity logic 14 for adding a parity bit to the response code 23. A second serialiser 15 translates the response code 23 into a response bit stream 24. The response bit stream 24 is placed on the serial link 3 by a second line driver 16. In the display adapter 92, a first receiver 17 detects the response bit stream 24 on the serial link 3. A first deserialiser 18 translates the detected response bit stream 24 back into the response code 23 which is decoded by the device driver 1.

The first serialiser and the first deserialiser of the adapter logic can be combined in a single integrated circuit module, and a similar module can be used to implement the second serialiser and the second deserialiser. The first line driver and the first receiver can also be incorporated in a single integrated module, and a similar driver/receiver module can be used to implement the second line driver and the second receiver.

The adapter logic 96 can be configured to receive a response from the device logic 97 in either a "Handshaking" mode or a "Data-streaming" mode. In the "Handshaking" mode, the device logic 97 waits for the adaptor logic to place an acknowledgement code on the serial link 3 before sending the next byte of the response. In the

"Data-streaming" mode, the device logic 97 waits for the adapter logic 96 to acknowledge receiving a block of bytes of the response before sending the next block.

An example of the present invention has been described wherein display information is communicated between the display adapter 92 and the display device 88 by communication logic 95 comprising a serial link 3 which is separate from the lines carrying the video and sync signal from the display adapter 92 to the display device. It will be appreciated however that other communication links and coding methods may be used. Furthermore, the example of the present invention includes a raster-scanned display device. It will be appreciated that the present invention is equally applicable to other display devices such a Liquid Crystal Display devices or vector-scanned display devices.

Claims

1. A display device (88) for connection to a display adaptor circuit (92) of a computer system, the display device comprising:

   means for generating a visual output in response to a plurality of data signals generated by the display adaptor circuit (92);

   characterised in that the display device (88) comprises:

   a memory (9) to store control data in the form of a plurality of control codes identifying the display device (88); and

   device logic means (97) responsive to a command signal from the display adaptor circuit (92) to read control codes from the memory (9) for transfer to the display adaptor circuit (92).

2. A display device as claimed in claim 1, comprising:

   a serial data link (3) for communicating the control code between the display device and the adaptor logic circuit.

3. A display device as claimed in claim 2 wherein the device logic means comprises a second receiver for receiving a command bit stream (22) from the adaptor logic circuit along the serial link, a deserialiser for translating the command bit stream (22) into the command signal (21), a command decoder for translating the command signal (21) into a memory address for accessing the stored control code, a serialiser for translating the control code into the control bit stream, and a line driver connected for communicating the control bit stream to the adaptor logic circuit along the serial link.

4. A display device as claimed in claim 3 wherein the serialiser and the deserialiser are combined in a single integrated circuit module.

5. A display device as claimed in claim 3 or claim 4 wherein the line driver and the receiver are incorporated in the a single integrated circuit module.

6. A display device as claimed in claim 2 and further comprising means for configuring the display device to operate in different display modes in response to mode control signals communicated from the adapter logic circuit to the device logic means along the serial link.

7. A display device as claimed in claim 2 or claim 6 and further comprising means for adjusting operating parameters of driver circuitry of the display device in response to parameter control signals communicated from the adapter logic circuit to the device logic means along the serial link.

8. A display device as claimed in claim 7 and further comprising means for obtaining digital samples of signals at nodes of the drive circuitry and for communicating the samples from the device logic means to the adapter logic circuit along the serial link in response to a data request signal communicated from the adapter logic circuit to the device logic means along the serial link.

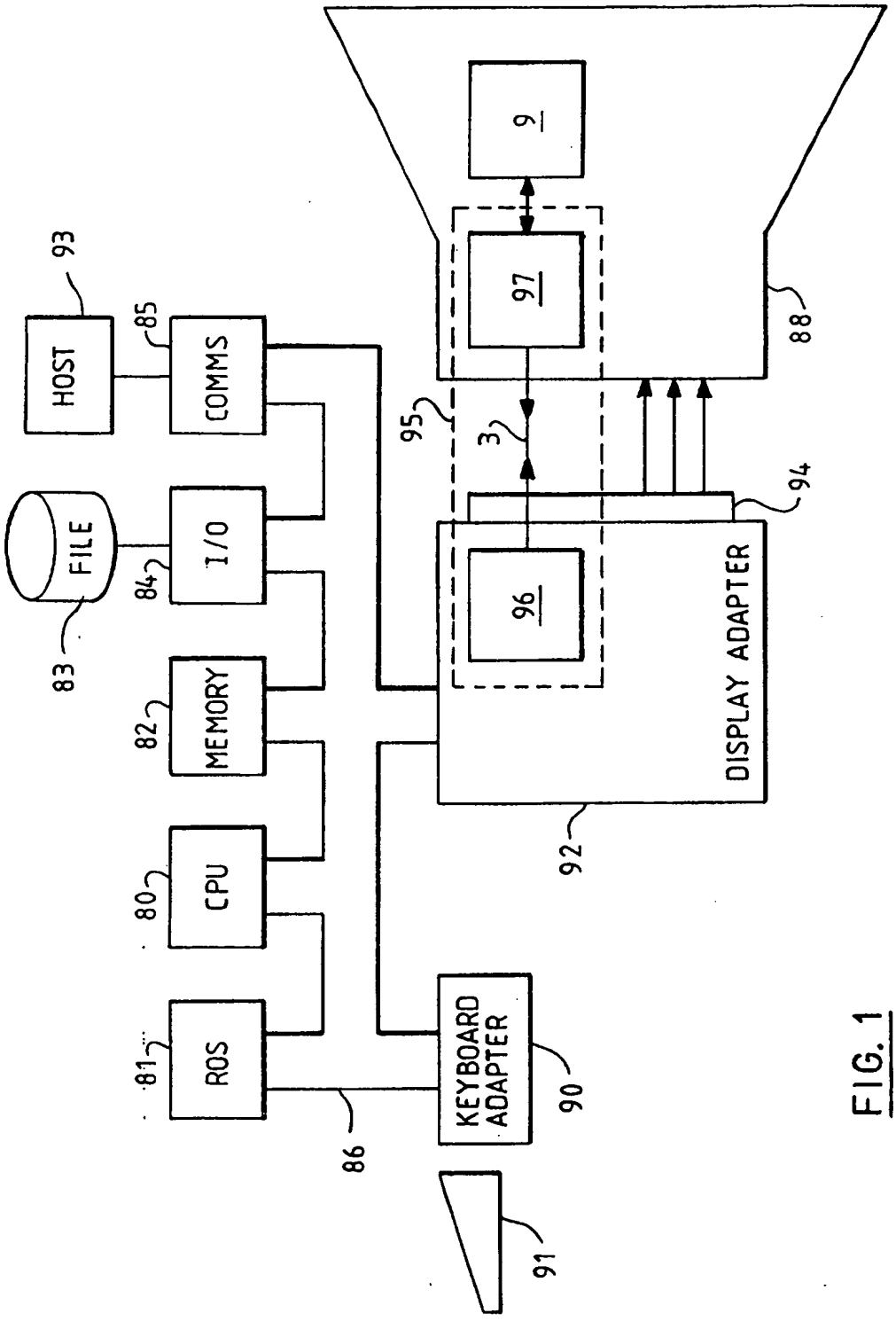
9
97
96
3
95
94
88
DISPLAY ADAPTER
92
HOST
93
COMMS
85
FILE
83
I/O
84
MEMORY
82
CPU
80
ROS
81
KEYBOARD ADAPTER
90
86
91

FIG. 1

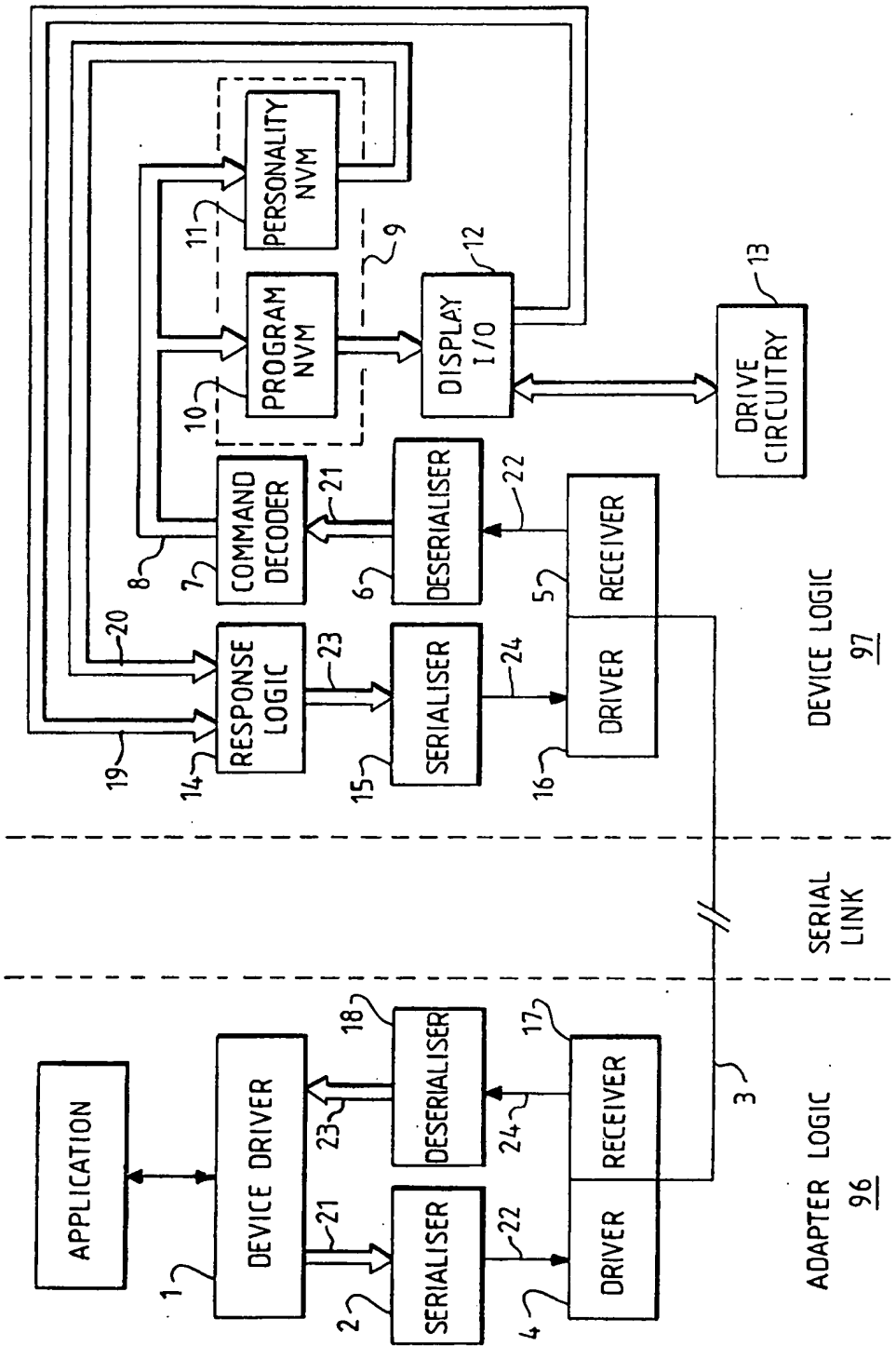
APPLICATION
DEVICE DRIVER
SERIALISER
DESERIALISER
DRIVER
RECEIVER
ADAPTER LOGIC
96
SERIAL LINK
DEVICE LOGIC
97
RESPONSE LOGIC
COMMAND DECODER
PROGRAM NVM
PERSONALITY NVM
DISPLAY I/O
DRIVE CIRCUITRY
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FIG. 2